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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,870	12/26/2001	Dongxing Jin	78945-24 /jlo	7587

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,870	JIN ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 15-25, 37-40* is/are rejected.

7)☒ Claim(s) *9-14,26-36,41 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations cited in claims 9-14, 26-36, and 41-42 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 15-25, and 37-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakai et al. (U.S. 6,115,728).

Re claim 1, Nakai et al. disclose in Figures 31-34 a method of performing a k-stage FFT (fast Fourier transform) computation of N data points wherein k and N are integers (e.g. N = 8 and k = 3 in Figure 32(b)), the method comprising: performing a plurality of operations upon the N data points (as label in Figure 32(b) as radix-2 decimation in frequency), each one of the plurality of operations comprising; performing an import of a respective plurality of sets of data points of the N data points from an external memory into an internal memory (e.g. transferring data from 11 to 12 in Figure 36); performing a FFT computation of the k-stage computation (as seen in Figure 32(b) with Figure 31 as structure) upon each one of the sets of data points in the internal memory (101 and 102 in Figure 31); and performing an export the respective plurality of sets of data points of the N data points from the internal memory into the external memory to update the respective sets of data points of the N data points in the external memory (e.g. output of data from 101 and 102 in Figure 31 and col. 3 lines 42-52).

Re claim 2, it has all limitations cited in claim 1 above. Thus, these limitations are rejected under the same rationale as cited in the rejection above. In addition, Nakai et

al. further disclose in Figure 13 a method of performing a k-stage FFT computation data points wherein k and N are integers (e.g. N = 8 and k = 3 in Figure 32(b)), the method comprising: for each one a plurality stage groupings of at least one stage of k stages of the k-stage FFT computation wherein the plurality of stage groupings of at least one stage collectively comprise the k stages (e.g. half portion of Figure 13 which contains all the stages), performing a respective plurality of operations on the N data points, each one of the respective plurality of operations.

Re claim 3, Nakai et al. further disclose a performing an import of a next respective plurality of sets of data points of the N data points for a next one of the respective plurality of operations while the performing computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory (col. 4 lines 25-40 as e.g. for processing data from RAM 101 and 102 using 303).

Re claim 4, Nakai et al. further disclose in Figure 31 performing an export previous respective plurality of sets of data points of the N data points for a previous one of the respective plurality of operations while the performing a FFT computation upon each one of the respective plurality of sets of data points of the N data points in the internal memory (col. 4 lines 25-40 as e.g. for updating existing data in RAM 101-102 from 303 and output to external memory through 121).

Re claim 5, Nakai et al. further disclose in Figure 31 the FFT computation is performed using decimation in frequency (DIF) (e.g. 341 and col. 3 lines 60-65).

Re claim 6, Nakai et al. further disclose in Figure 31 the FFT computation is performed using decimation in time (DIT) (e.g. 342 and col. 3 lines 60-65).

Re claim 7, Nakai et al. further disclose in Figure N substantially satisfies $N = 2^k$ (e.g. N = 8 and k = 3 in Figure 32(b)).

Re claim 8, Nakai et al. further disclose in Figures 13 and 32(b) the stage groupings of at least one stage comprise Q stage groupings each comprising S stages, Q and S being integers with Q>=l, S>=1 and k>=QS (e.g. Q = 1; S = 3; and k = 3).

Re claim 15, Nakai et al. further disclose in Figures 13 and 32(b) the stage groupings of at least one stage comprise a stage grouping comprising D stages wherein D is an integer and k=QS+D (e.g. D = 0).

Re claim 16, Nakai et al. further disclose in Figures 13 and 32(b) the performing an import comprises importing the plurality of sets of data points into buffer in the internal memory, the buffer having a capacity to hold M_I data points and D being an integer substantially satisfying $D<=\log2(M_I)$ (inherently since D is set to 0 therefore M_I can be anything larger than 0).

Re claim 17, Nakai et al. further disclose in Figures 13 and 32(b) the performing an import comprises importing the plurality of sets of data points into one of two buffers of a double buffer in the internal memory, each one of the two buffers having a capacity to hold $M_I/2$ data points and D being an integer substantially satisfying $D<=1og2(M_I/2)$ (inherently since D is set to 0 therefore $M_I/2$ can be anything larger than 0).

Re claim 18, Nakai et al. further disclose in Figures 13 and 32(b) for each one of a plurality of sub-stage groupings of at least one stage of the stage grouping of D stages wherein the plurality of sub-stage groupings of least one stage collectively comprise the D stages (Figure 13), performing a set of sub-stage FFT computations wherein each one

of the sub-stage FFT computations respective data points and respective twiddle factors (304) are loaded into a high- speed cache.

Re claim 19, it is a processing platform claim of claim 2. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 20, it is a processor claim of claim 2. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 21, it is a processor claim of claim 2. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 22, Nakai et al. further disclose in Figures 34 and 36 at least one bus wherein the DMA unit is further adapted to import the respective plurality of sets of data points, of the N data points, from the external memory and to export the respective plurality of sets of data points, of the N data points, into the external memory through the at least one bus (e.g. the external memory is located in 11 through a bus to 12 in Figure 36).

Re claim 23, Nakai et al. further disclose in Figures 34 and 36 the double buffer comprising two buffers each adapted to stored data points (405 and 406); two buses (403 and 404) each adapted to provide a channel for importing the data points into a respective one of the two buffers (405 and 406) and for exporting the data points from the respective one of the two buffers; and the CPU (402) being further adapted to provide instructions to the DMA unit for importing a respective plurality of sets of data points, of the N data points, into one of the two buffers (as seen in Figure 31 with RAM 101 and 102) while

the CPU performs FFT computations upon another respective plurality of sets of data points, of the N data points, stored in another one of the two buffers (col. 24 lines 11-21).

Re claim 24, Nakai et al. further disclose in Figures 34 and 36 the internal memory comprises: double buffer (405 and 406) comprising two buffers each adapted to stored data points; two buses (403 and 404) each adapted to provide a channel for importing the data points into a respective one of the two buffers (405 and 406) and for exporting the data points from the respective one of the two buffers; and the CPU (402) being further adapted to provide instructions to the DMA unit for exporting respective sets of data points from one of the two buffers while the CPU performs computations upon other respective sets of data points stored in another one of the two buffers (col. 24 lines 11-21).

Re claim 25, it is a processor claim of claim 8. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 37, Nakai et al. further disclose in Figures 34 and 36 the CPU is adapted to produce the k-stage FFT computation in real-time (Figures 32(a) and 36).

Re claim 38, Nakai et al. further disclose in Figure 31 the internal memory comprises a buffer (304) adapted store twiddle factors used in the FFT computations.

Re claim 39, it is an article manufacture claim of claim 1. Thus, claim 39 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 40, Nakai et al. further disclose in Figures 34 and 36 the stage groupings of at least one stage comprise a stage grouping of D stage and Q stage groupings of S

stages wherein D, Q, and S are integers and wherein k substantially satisfies k =QS+D and k = log(N) (e.g. Q = 1; S = 3; and k = 3 wherein D = 0; k = 3 as $\log_2(8)$).

Allowable Subject Matter

4. Claims 9-14, 26-36, and 40-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,029,079 to Magar et al. disclose an apparatus and method for flexible control of digital signal processing devices.

b. U.S. Patent No. 5,091,875 to Wong et al. disclose a fast fourier transform addressing apparatus and method.

c. U.S. Patent No. 6,421,696 to Horton discloses a system and method for high speed execution of fast fourier transforms utilizing SIMD instructions on a general purpose processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

October 21, 2004

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2124